IN THE CLAIMS

The Claims have been amended as follows:

1. (Currently Amended) An apparatus comprising:

at least two sampling circuits to sample incoming data and a first clock;

a clock generation unit to generate a plurality of sampling clocks from a second clock, the plurality of sampling clocks used by ~~the sampling circuits~~ the at least two sampling circuits to sample the incoming data and the first clock;

a phase detector to detect a phase difference between the first clock and the second clock; and

a delay line to delay the sampled incoming data based on the detected phase difference, wherein the delay line delays the sampled incoming data by selecting one of sampled data points of the sampled incoming data.

2. (Original) A method of data resynchronization comprising:

(a) sampling incoming data and a first clock;

(b) generating at least three sampling clocks from a second clock, each of the three sampling clocks to sample the incoming data and the first clock;

(c) detecting a phase difference between the first clock and the second clock; and

(d) delaying the sampled incoming data based on the detected phase difference by selecting one of sampled data points of the sampled incoming data.